

SYNCHRONIZING METHOD AND APPARATUSCROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is the first application filed for the present invention.

TECHNICAL FIELD

[0002] This invention relates to the field of telecommunications. More precisely, this invention pertains to a method and apparatus for synchronizing a burst or a packet transmission signal.

BACKGROUND OF THE INVENTION

[0003] In Orthogonal Frequency Division Multiplexing (OFDM), various methods are known and used for performing a synchronization of a signal with a known sequence.

[0004] For packet transmission, such as in wireless LAN IEEE 802.11 systems or broadband wireless access IEEE 802.16a systems, an efficient method involves transmitting particular OFDM symbols which are known to a receiver.

[0005] Now referring to Fig. 1, there is shown an embodiment of a prior art synchronizer. The synchronizer performs a synchronization of an incoming series of complex samples of an incoming signal with a known sequence of a plurality of coefficients  $C_0 \dots C_n$  which represent a pattern within the incoming signal, known to the synchronizer.

[0006] The prior art synchronizer comprises a plurality of delay units 10, a plurality of multipliers 12, an adding unit 14 and a maximum finding unit 16.

**[0007]** Each delay unit 10 of the plurality of delay units 10 delays a corresponding incoming series of complex samples of the incoming signal by a fixed delay.

**[0008]** Each multiplier 12 of the plurality of multipliers 12 multiplies a corresponding signal with a corresponding coefficient of the sequence of the plurality of coefficients to provide a corresponding multiplied signal.

**[0009]** The adding unit 14 receives each of the multiplied signals and provides an added signal which is equal to the sum of each of the multiplied signals.

**[0010]** The maximum finding unit 16 receives the added signal and provides a synchronization signal when the added signal satisfies criteria for identifying a maximum.

**[0011]** Someone skilled in the art will appreciate that the maximum value signal is outputted in the case where the incoming input signal matches the sequence of the plurality of coefficients.

**[0012]** Unfortunately, as will be appreciated by someone skilled in the art, such embodiments may be dependent on various parameters which may affect ultimately the maximum value signal provided by the maximum finding unit 16. For instance, the signal may be affected by noise or the amplitude of the signal may be attenuated.

**[0013]** It will also be appreciated by the skilled addressee that a multiplier of the plurality of multipliers 12 is costly to implement in hardware, especially in the case of a

Field Programmable Gate Array (FPGA) or in the case of an Application Specific Integrated Circuit (ASIC).

[0014] In view of the above, there is a need for a method and apparatus that will overcome the above-identified drawbacks and that will further be less complex to implement.

#### **SUMMARY OF THE INVENTION**

[0015] It is an object of the invention to provide a method for synchronizing a burst with a known sequence of at least one coefficient.

[0016] Yet another object of the invention is to provide an apparatus for synchronizing a burst with a known sequence of at least one coefficient.

[0017] According to a first aspect of the invention, there is provided, in a communication device, a method of synchronizing at least one known coefficient to a transmitted signal having an arbitrary power value, the method comprising determining a quantization bit indicative of the arbitrary power value, correlating the quantization bit with the at least one known coefficient to obtain a correlated signal, selecting the correlated signal when the correlated signal matches a given criterion, synchronizing the transmitted signal with the at least one known coefficient using the selected correlated signal.

[0018] According to another aspect of the invention, there is provided, in a communication device, a synchronizer for synchronizing a known sequence of coefficients, the sequence of coefficients having a real part and an imaginary part, to

an incoming input signal, the incoming input signal having a real part and an imaginary part, comprising a first correlation unit correlating the imaginary part of the incoming input signal with the imaginary part of the sequence of at least one coefficient to provide a first correlated signal, a second correlation unit correlating the real part of the incoming input signal with the real part of the sequence of at least one coefficient to provide a second correlated signal, a third correlation unit correlating the imaginary part of the incoming input signal with the real part of the sequence of at least one coefficient to provide a third correlated signal, a fourth correlation unit correlating the real part of the incoming input signal with the imaginary part of the sequence of at least one coefficient to provide a fourth correlated signal, a first adding unit subtracting the first correlated signal and the second correlated signal to "4" to provide a first added signal, a second adding unit subtracting the third correlated signal and adding the fourth correlated signal to provide a second added signal and a criterion matching unit determining which of the first added signal and the second added signal matches a given criterion.

**[0019]** According to another aspect of the invention, there is provided, in a communication system, a synchronizer for determining when a transmitted signal, having an arbitrary power value, matches at least one known coefficient, the synchronizer comprising a quantizer determining a quantization bit indicative of the arbitrary power value, a correlator to correlate the quantization bit with the at least one known coefficient to obtain a correlated signal, a

selector to select the correlated signal when the correlated signal matches a given criterion.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0020]** Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the appended drawings, in which:

**[0021]** Fig. 1 is a schematic which shows a prior art synchronizer;

**[0022]** Fig. 2 is a schematic which shows a synchronizer which performs a synchronization of an incoming input signal with a sequence of at least one coefficient according to the preferred embodiment of the invention;

**[0023]** Fig. 3 is a flowchart which shows the preferred embodiment of the invention; according to a first step, an incoming input signal is provided, a sequence of at least one coefficient is then provided and the incoming input signal provided is synchronized with the sequence of at least one coefficient;

**[0024]** Fig. 4 is a flowchart which shows how the incoming input signal is provided;

**[0025]** Fig. 5 is a flowchart which shows how the sequence of at least one coefficient is provided;

**[0026]** Fig. 6 is a flowchart which shows how synchronization is achieved between the incoming input signal and the

sequence of at least one coefficient in the preferred embodiment of the invention; and

[0027] Fig. 7 is a schematic which shows a synchronizer which performs a synchronization of an incoming input signal with a sequence of a plurality of coefficients according to the preferred embodiment of the invention.

[0028] It will be noted that throughout the appended drawings, like features are identified by like reference numerals.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0029] Now referring to Fig. 3, there is shown how the synchronizer 17 operates in the preferred embodiment of the invention.

[0030] According to step 20, an incoming input signal to synchronize with a sequence of at least one coefficient is provided to the synchronizer.

[0031] According to step 22, the sequence of at least one coefficient is provided to the synchronizer 17.

[0032] According to step 24, the provided incoming input signal is synchronized with the provided sequence of at least one coefficient.

[0033] Now referring to Fig. 4, there is shown how the signal to synchronize, according to step 20, is provided in one embodiment of the invention.

[0034] According to step 30, the incoming input signal is received by the synchronizer. In the preferred embodiment of the invention, the incoming input signal comprises a real part and an imaginary part.

[0035] According to step 32, the real part of the incoming input signal is extracted.

[0036] According to step 34, the imaginary part of the incoming input signal is extracted.

[0037] According to step 36, signum of the extracted real part of the incoming input signal is computed.

[0038] While someone skilled in the art will appreciate that signum (Sgn()) function is usually defined as follows for a function  $f$ :

[0039]  $\text{Sgn}(f)=1$  if  $f>0$ ;

[0040]  $\text{Sgn}(f)=0$  if  $f=0$ ; and

[0041]  $\text{Sgn}(f)=-1$  if  $f<0$ , it will be appreciated in the following that the signum function used in the preferred embodiment described herein is defined as follows:

[0042]  $\text{Sgn}(f)=1$  if  $f\geq 0$ ;

[0043]  $\text{Sgn}(f)=-1$  if  $f<0$ .

[0044] According to step 37, signum of the extracted imaginary part of the incoming input signal is computed.

**[0045]** Now referring to Fig. 5, there is shown how the sequence of at least one coefficient is provided according to step 22.

**[0046]** According to step 40, the sequence of at least one coefficient is received by the synchronizer. In the preferred embodiment of the invention, the sequence of at least one coefficient comprises a real part and an imaginary part.

**[0047]** According to step 42, the real part of the sequence of at least one coefficient is extracted.

**[0048]** According to step 44, the imaginary part of the sequence of at least one coefficient is extracted.

**[0049]** According to step 46, signum of the extracted real part of the sequence of at least one coefficient is computed.

**[0050]** According to step 47, signum of the extracted imaginary part of the sequence of at least one coefficient is computed.

**[0051]** Now referring to Fig. 6, there is shown how the synchronization is achieved between the provided incoming input signal and the sequence of at least one coefficient according to step 24 in the preferred embodiment of the invention.

**[0052]** According to step 50, a mapped signum of the real part of the incoming input signal is provided. In fact, the signum of the real part of the incoming input signal, which is computed according to step 36, is mapped. Preferably, the signum of the real part of the incoming input signal is



mapped in order to be located at 0 and 1 rather than to be located at -1 and 1.

**[0053]** According to step 52, a mapped signum of the imaginary part of the incoming input signal is provided. The signum of the imaginary part of the incoming input signal, which is computed according to step 37, is mapped. Preferably, the signum of the imaginary part of the incoming input signal is mapped in order to be located at 0 and 1 rather than to be located at -1 and 1.

**[0054]** According to step 54, a mapped signum of the real part of the sequence of at least one coefficient is provided. The signum of the real part of the sequence of at least one coefficient, which is computed according to step 46, is mapped. Preferably, the signum of the real part of the sequence of at least one coefficient is mapped in order to be located at 0 and 1 rather than to be located at -1 and 1.

**[0055]** According to step 56, a mapped signum of the imaginary part of the sequence of at least one coefficient is provided. The signum of the imaginary part of the sequence of at least one coefficient, which is computed according to step 47, is mapped. Preferably, the signum of the imaginary part of the sequence of at least one coefficient is mapped in order to be located at 0 and 1 rather than to be located at -1 and 1.

**[0056]** According to step 58, an exclusive or (XOR) operation is performed using the mapped signum of the real part of the signal, the mapped signum of the imaginary part of the signal, the mapped signum of the real part of the sequence of

at least one coefficient and the mapped signum of the imaginary part of the sequence of at least one coefficient. A cross-correlated result signal is provided upon completion of the exclusive or (XOR) operation.

[0057] Someone skilled in the art will appreciate that such exclusive or (XOR) operation is of great advantage as it is very easy to implement in hardware.

[0058] According to step 60, a sum is computed using the result of the exclusive or (XOR) operation performed in step 58.

[0059] According to step 62, a maximum in the cross-correlated signal is located using the result of the sum computed according to step 60. In the preferred embodiment, the maximum is located by detecting the maximum of  $p = y^*(n) \cdot y(n)$ , where  $y(n)$  is the cross-correlated signal.

[0060] It will be appreciated that detecting the maximum in the cross correlated signal is a specific case of a more general embodiment where step 62 is achieved when the cross-correlated signal matches a given criterion. Such given criterion may be provided depending on an application. In fact, it will be appreciated that in the case where some noise is added to the signal, finding the maximum may not be reliable. Alternatively, the given criterion may be defined using statistical parameters for instance.

[0061] Now referring to Fig. 2, there is shown a synchronizer 17 in one embodiment of the invention.

**[0062]** In this embodiment, an incoming input signal  $G$ , having an arbitrary power value, is provided to the synchronizer. The incoming input signal  $G$  comprises a real part  $\text{Re}(G)$  and an imaginary part  $\text{Im}(G)$ .

**[0063]** The synchronizer 17 synchronizes the incoming input signal  $G$  with a sequence of at least one coefficient  $C$ . In this embodiment, the sequence comprises one coefficient. The sequence of at least one coefficient comprises a real part  $\text{Re}(C)$  and an imaginary part  $\text{Im}(C)$ .

**[0064]** The synchronizer 17 comprises a first correlation unit 18 which correlates the imaginary part of the incoming input signal  $\text{Im}(G)$  with the imaginary part of the sequence of at least one coefficient  $\text{Im}(C)$  to provide a first correlated signal.

**[0065]** The synchronizer 17 comprises a second correlation unit 18 which correlates the real part of the incoming input signal  $\text{Re}(G)$  with the real part of the sequence of at least one coefficient  $\text{Re}(C)$  to provide a second correlated signal.

**[0066]** The synchronizer 17 comprises a third correlation unit 18 which correlates the imaginary part of the incoming input signal  $\text{Im}(G)$  with the real part of the sequence of at least one coefficient  $\text{Re}(C)$  to provide a third correlated signal.

**[0067]** The synchronizer 17 comprises a fourth correlation unit 18 which correlates the real part of the incoming input signal  $\text{Re}(G)$  with the imaginary part of the sequence of at least one coefficient  $\text{Im}(C)$  to provide a fourth correlated signal.

**[0068]** The synchronizer 17 further comprises a first adding unit 14. The first adding unit 14 subtracts the first correlated signal and the second correlated signal to 4 to provide a first added signal.

**[0069]** The synchronizer 17 further comprises a second adding unit 14. The second adding unit 14 subtracts the third correlated signal and adds the fourth correlated signal to provide a second added signal.

**[0070]** The synchronizer 17 further comprises the maximum finding unit 16 which determines which of the first added signal and the second added signal provides a maximum value. Someone skilled in the art will appreciate that it is then possible to synchronize the incoming input signal G with the sequence of at least one coefficient C when the maximum value is located according to step 62 of Fig. 6. It will further be appreciated that the maximum finding unit 16 is a specific case of a criterion matching unit.

**[0071]** Now referring to Fig. 7, there is shown a schematic of a synchronizer which performs a synchronization of an incoming input signal with a sequence of a plurality of coefficients according to the preferred embodiment of the invention.

**[0072]** The synchronizer comprises a plurality of correlation units 18, a plurality of delay units 15, a plurality of adding units 14 and a maximum finding unit 16.

**[0073]** The plurality of correlation units 18, the plurality of adding units 14 and the maximum finding unit 16 function in the same manner as described with Fig. 2.

[0074] Each delay unit of the plurality of delay units 15 is used to delay an incoming signal by a predetermined delay.

[0075] The result of a cross-correlation of the sequence of a plurality of coefficients with the incoming input signal is

$$\begin{aligned}
 y(n) &= \sum_{i=0}^{N-1} c(i)^* * g(i+n) \\
 [0076] \quad &= \sum_{i=0}^{N-1} [\operatorname{Re}\{c(i)\} \operatorname{Re}\{g(i+n)\} + \operatorname{Im}\{c(i)\} \operatorname{Im}\{g(i+n)\}] \\
 &\quad + j \sum_{i=0}^{N-1} [\operatorname{Re}\{c(i)\} \operatorname{Im}\{g(i+n)\} - \operatorname{Im}\{c(i)\} \operatorname{Re}\{g(i+n)\}]
 \end{aligned}$$

[0077] where  $c(i)$  are the plurality of complex coefficients,  $g(i)$  are complex samples of the incoming input signal,  $N$  is the number of coefficients of the sequence,  $i$  is the coefficient index and  $n$  is the sample index.

[0078] A signum of the last equation provides that

$$\begin{aligned}
 y(n) &= \sum_{i=0}^{N-1} [\operatorname{sign}\{\operatorname{Re}\{c(i)\}\} \operatorname{sign}\{\operatorname{Re}\{g(i+n)\}\} + \operatorname{sign}\{\operatorname{Im}\{c(i)\}\} \operatorname{sign}\{\operatorname{Im}\{g(i+n)\}\}] \\
 [0079] \quad &\quad + j \sum_{i=0}^{N-1} [\operatorname{sign}\{\operatorname{Re}\{c(i)\}\} \operatorname{sign}\{\operatorname{Im}\{g(i+n)\}\} - \operatorname{sign}\{\operatorname{Im}\{c(i)\}\} \operatorname{sign}\{\operatorname{Re}\{g(i+n)\}\}]
 \end{aligned}$$

[0080] The last equation may be expressed as:

$$[0081] \quad y(n) = \sum_{i=0}^{N-1} [m_{RR}(i, n) + m_{II}(i, n)] + j \sum_{i=0}^{N-1} [m_{RI}(i, n) - m_{IR}(i, n)],$$

[0082] where

$$\begin{aligned}
[0083] \quad m_{RR}(i, n) &\equiv \text{sign}\{\text{Re}\{c(i)\}\}\text{sign}\{\text{Re}\{g(i+n)\}\} \\
m_{II}(i, n) &\equiv \text{sign}\{\text{Im}\{c(i)\}\}\text{sign}\{\text{Im}\{g(i+n)\}\} \\
m_{RI}(i, n) &\equiv \text{sign}\{\text{Re}\{c(i)\}\}\text{sign}\{\text{Im}\{g(i+n)\}\} \\
m_{IR}(i, n) &\equiv \text{sign}\{\text{Im}\{c(i)\}\}\text{sign}\{\text{Re}\{g(i+n)\}\}
\end{aligned}$$

[0084] A mapping is then performed in order to have a result of a signum being one of 0 and 1, rather than being one of -1 and 1. To achieve such result, it is necessary that:

$$[0085] \quad x_o = 1 - 2x_n .$$

[0086] With the expressions:

$$\begin{aligned}
[0087] \quad b_{RR}(i, n) &\equiv \frac{1 - m_{RR}(i, n)}{2} \\
b_{II}(i, n) &\equiv \frac{1 - m_{II}(i, n)}{2} \\
b_{RI}(i, n) &\equiv \frac{1 - m_{RI}(i, n)}{2} , \text{ it is possible to show that} \\
b_{IR}(i, n) &\equiv \frac{1 - m_{IR}(i, n)}{2}
\end{aligned}$$

$$\begin{aligned}
[0088] \quad y(n) &= \sum_{i=0}^{N-1} [1 - 2b_{RR} + 1 - 2b_{II}] + j \sum_{i=0}^{N-1} [1 - 2b_{RI} - (1 - 2b_{IR})] \\
&= 2 \sum_{i=0}^{N-1} [1 - b_{RR} - b_{II}] + 2j \sum_{i=0}^{N-1} [b_{IR} - b_{RI}] \\
&= 2N - 2 \sum_{i=0}^{N-1} b_{RR} - 2 \sum_{i=0}^{N-1} b_{II} + 2j \left[ \sum_{i=0}^{N-1} b_{IR} - \sum_{i=0}^{N-1} b_{RI} \right]
\end{aligned}$$

[0089] which may be simplified as

$$[0090] \quad y(n) = N - \sum_{i=0}^{N-1} b_{RR} - \sum_{i=0}^{N-1} b_{II} + j \left[ \sum_{i=0}^{N-1} b_{IR} - \sum_{i=0}^{N-1} b_{RI} \right]$$

[0091] The above-identified formula is therefore implemented in Fig. 7.

[0092] Someone skilled in the art will appreciate that such embodiment enables performing exclusive-OR which is of great advantage as the exclusive-OR, performed in units 18 of Figs. 2 and 7, is easy to implement in hardware. It will further be appreciated that only one bit is used for quantization. Such one-bit quantization is of great advantage as signum function is not dependent on the amplitude of the signal but rather on the sign value of the input power of the signal.

[0093] The maximum finding unit 16 operates by finding a peak in the amplitude or amplitude-squared component of  $y(n)$ .

[0094] More precisely, the peak is equal to:

[0095] 
$$p(n) = y(n) \cdot y(n)^*$$

[0096] In one embodiment, the maximum finding unit 16 operates by finding a maximum which is located when the sequence of the plurality of coefficients  $C_0 \dots C_n$  matches the coefficients in an input signal.

[0097] Alternatively, the maximum finding unit 16 operates using a given criterion. The given criterion may be a threshold for instance. The threshold is chosen such that the probability of providing a false maximum is minimized while at the same time the probability of missing a valid trigger is sufficiently low. These conditions require estimating the probability distribution functions for the false synchronization and for a valid synchronization where the signal is distorted due to various impairments.

[0098] The embodiments of the invention described above are intended to be exemplary only. The scope of the invention is therefore intended to be limited solely by the scope of the appended claims.